

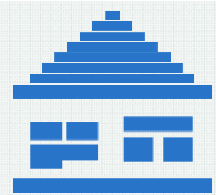


**Association for  
Computing Machinery**

# 2022 MICRO Test of Time Award

Presented by  
Aamer Jaleel

ACM SIGMICRO



# MICRO-55

IEEE/ACM International Symposium on Microarchitecture  
Chicago, IL, October 1-5 2022

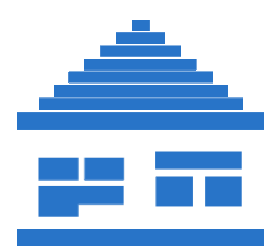
## MICRO Test of Time Award

**Recognizes an influential MICRO paper(s) whose impact is still felt 18–22 years after its initial publication.**

**This year, papers from MICRO 2000-2004 were eligible.**

# MICRO Test of Time Award Selection Committee

- Murali Annavaram (University of Southern California)
- Reetuparna Das (University of Michigan)
- Antonio Gonzalez (Universitat Politècnica de Catalunya)
- Sudhanva Gurumurthi (AMD)
- Aamer Jaleel (NVIDIA), *chair*
- Andre Seznec (Intel)
- Viji Srinivasan (IBM)



# MICRO-55

IEEE/ACM International Symposium on Microarchitecture  
Chicago, IL, October 1-5 2022

## *MICRO Test of Time Award*

Presented to:

***Canturk Isci and Margaret Martonosi***

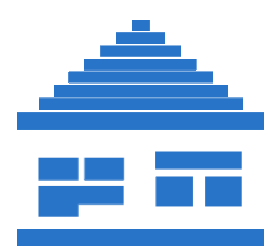
For the MICRO-2003 paper entitled:

### ***Runtime Power Monitoring in High-End Processors: Methodology and Empirical Data***

*For introducing a real-system hardware performance counter based power measurement and estimation methodology that enabled live per-block power dissipation estimates and that identified different power phases of application execution.*

**Onur Mutlu**  
SIGMICRO Chair

**Aamer Jaleel**  
Selection Committee Chair



# MICRO-55

IEEE/ACM International Symposium on Microarchitecture  
Chicago, IL, October 1-5 2022

## *MICRO Test of Time Award*

Presented to:

***Shubu Mukherjee, Christopher T. Weaver, Joel S. Emer, Steven K. Reinhardt, Todd M. Austin***

For the MICRO-2003 paper entitled:

### ***A Systematic Methodology to Compute the Architectural Vulnerability Factors for a High-Performance Microprocessor***

*For defining and estimating Architectural Vulnerability Factor (AVF) of processor structures using a novel approach that tracks the subset of state bits required for architecturally correct execution (ACE). ACE analysis, now an industry best practice, has allowed processor architects to reason about the impact of transient faults in a technology-independent manner and prioritize protection decisions early in the design cycle.*

**Onur Mutlu**  
SIGMICRO Chair

**Aamer Jaleel**  
Selection Committee Chair